A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast Electrode-Addressing EWOD Chips

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ABSTRACT

Electrowetting-on-dielectric (EWOD) chips have emerged as the most widely used actuators for digital microfluidic (DMF) systems. These devices enable the electrical manipulation of microfluidics with various advantages such as low power consumption, flexibility, accuracy, and efficiency. In addressing the need for low-cost and practical fabrication, pin-count reduction has become a key problem to the large-scale integration of EWOD-chip designs. One of the major approaches, *broadcast addressing*, reduces the pin count by assigning a single control pin to multiple electrodes with mutually compatible control signals. Most previous studies utilize this addressing scheme by scheduling fluidic-level synthesis on pin-constrained chip arrays. However, the associated interconnect routing problem is still not provided in currently available DMF automations, and thus the broadcast-addressing scheme cannot be actually realized. In this paper, we present the *first* network-flow based pin-count aware routing algorithm for EWOD-chip designs with a broadcast electrode-addressing scheme. Our algorithm simultaneously takes pin-count reduction and wirelength minimization into consideration for higher integration and better design performance. Experimental results show the effectiveness and scalability of our algorithm on a set of real-life chip applications.

1. INTRODUCTION

Due to the principle of electrowetting-on-dielectric (EWOD), the EWOD chip has been appreciated as a promising actuator for digital microfluidic (DMF) systems [11, 12, 13]. This chip enables the electrical manipulation of discrete fluidics (i.e., *droplets*) with low power consumption, flexibility, and efficiency. Furthermore, their capability of automatic and parallel controls offers faster and more precise execution. These advantages increase the practicality of applications including immunoassays, DNA sequencing, and point-of-care diagnosis on miniaturized DMF systems with lower cost, less reagent consumption, and higher immunity to human error.

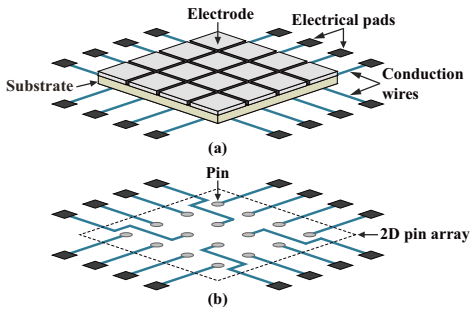

Figure 1: (a) Schematic view of an EWOD chip. (b) Routing model on a 2D pin array.

As schematically presented in Figure 1(a), the general diagram of a two-dimensional (2D) EWOD chip contains a patterned electrode array, conduction wires, electrical pads, and a substrate [6, 12, 13]. Through these electrical devices, external control circuits can drive these electrodes by assigning time-varying actuation voltage. Thus, by generating electrohydrodynamic force from electrodes, many fluidic-level controls can be performed due to the electrowetting phenomenon [11].

To correctly drive the electrodes, *electrode addressing* is introduced as a method through which electrodes are assigned or controlled by pins to identify input signals. Early EWOD-chip designs relied on *direct addressing* [6], where each electrode is directly and independently assigned by a dedicated control pin. This addressing maximizes the flexibility of electrode controls. However, for large arrays, the high pin-count demand complicates the electrical connections, thus rendering this kind of chip unreliable and prohibitively expensive to manufacture [15, 16].

Recently, *pin-constrained* design has been raised as a possible solution to this problem. One of the major approaches, *broadcast addressing*, reduces the number of control pins by assigning a single control pin to multiple electrodes with mutually compatible control signals [15]. In other words, multiple electrodes are controlled by a single control signal and are thus driven simultaneously. In this regard, much ongoing effort has been made to group sets of electrodes that can be driven uniformly without introducing signal conflict [14, 15].

For electrical connections, conduction wires must be routed from the topside electrode array, through the underlying substrate, to the surrounding pads. Hence, after the electrodes are addressed with control pins, the routing problem for EWOD chips can be specified to a 2D pin array, while establishing correspondence between control pins and pads (see Figure 1(b)). However, this routing issue is still not readily available among automations for EWOD chips, revealing an insufficiency of current DMF design tools. Due to the specialized electrode structure and control mechanism, it is desirable to develop a dedicated routing algorithm for EWOD chips, especially given the issue of the pin-constrained design.

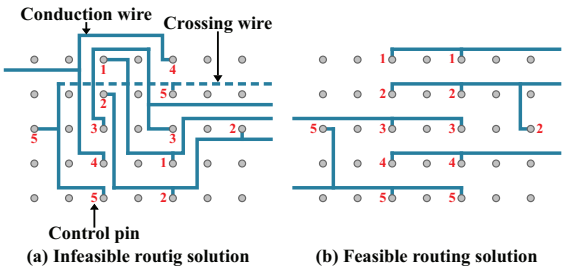

Figure 2: Comparison of two different design methods for performing the same fluidic controls. (a) Considers electrode addressing and routing separately. (b) Considers electrode addressing and routing simultaneously.

Furthermore, if routing is simply adopted to an electrode-addressing result, the feasibility and quality of routing solutions may inevitably be limited. For example, Figure 2 illustrates two routing solutions under two different design methods that perform the same fluidic controls. In (a), the separate consideration of electrode addressing and routing results in many back detours for pins 3-4, and thus blocks the routing for pin 5. On the other hand, in (b), simultaneous consideration of electrode addressing and routing provides a higher feasibility and quality routing solution in terms of routability and wirelength. In the case of (a), additional post processes such as electrode readdressing and rerouting should be further included, and thus the effectiveness of the entire design may be quite restricted.

Given these concerns, it is necessary to develop an integrated design automation to assist in these practical design issues. Consequently, we propose in this paper a pin-count aware routing algorithm that simultaneously considers electrode addressing and routing to achieve greater design flexibility and higher design performance.

1.1 Previous Work

To the best knowledge of the authors, there is no previous work in the literature that provides a general pin-count aware routing algo-

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rithm for EWOD chips. Most related works focus on pin-constrained electrode-addressing methods [9, 14, 15]. The work by [14] proposes an array-partition based method to group the electrode set without introducing unexpected fluidic-level behaviors. The work by [15] presents a clique-partition based algorithm to formulate compatibility between control signals. By recognizing a minimum clique partition, the required control pins can be optimized. However, since the minimum clique partition is well-known as an NP-hard problem, a heuristic method of iterative clique recognitions is also proposed. The work by [9] further integrates various pin-count saving techniques into fluidic-level synthesis, and then systematically addresses electrodes according to pre-classified categories of pin demand. Although these state-of-the-art works can address the electrodes with fewer and fewer control pins to correctly perform the scheduled fluidic functions, the associated routing problem is still not considered. Recent work by [16] applies a Connect-5 algorithm to group the electrode set and briefly discusses the routing problem. Nevertheless, this method depends on a special architecture of electrical connections (i.e., multiple conducting layers and slanted routes), and a means for adopting a specific routing algorithm for a general EWOD-chip design is still not provided.

1.2 Our Contributions

In this paper, we propose a novel pin-count aware routing algorithm for broadcast electrode-addressing EWOD chips. Compared with prior design automations, our router is the *first* work in the literature that provides integrated electrode addressing and routing for general chip architectures. Considering both the issues of pin-constrained design and practical routing requirements, our method can simultaneously minimize the required number of control pins and wirelength to achieve better design performance.

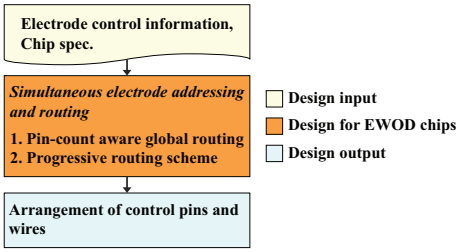


Figure 3: Our routing algorithm for the EWOD-chip design.

As summarized in Figure 3, we adopt a two-stage technique of pin-count aware global routing followed by a progressive routing scheme to simultaneously consider the electrode addressing and routing problems. Two kinds of flow networks, *maximum-flow formulation* and *minimum-cost maximum-flow formulation*, are respectively introduced in each stage to effectively and correctly solve the electrode addressing and routing problems. Along with the design flows and algorithms, our contributions include the followings:

- We propose the *first* design algorithm to deal with the routing problem on broadcast electrode-addressing EWOD chips. We comprehensively integrate various pin-count saving issues into our two-stage routing technique to reduce the required number of control pins, while keeping the wirelength minimized.
- In *pin-count aware global routing*, we derive a *maximum-flow formulation* with the duality of min-cut property to construct the global routing tracks. By guiding horizontal/vertical routes on these specific tracks, the pin count and wirelength can be simultaneously minimized in a global view.
- In the *progressive routing scheme*, we divide the original routing problem into a set of manageable subproblems corresponding to each pin-count expansion. By deriving a *minimum-cost maximum-flow network* to formulate the pin-count expansion, the required number of control pins can be minimally determined for electrode addressing and routing in each subproblem.

Experimental results demonstrate the scalability and effectiveness of our algorithm. The evaluation performed on a set of real-life chip applications shows that our algorithm achieves the best results in terms of routability, pin-count demand, and wirelength. We also simulate the fluidic-level synthesis and randomly generate several hard test designs to show the robustness of our algorithm.

The remainder of this paper is organized as follows. Section 2 describes the related preliminaries. Section 3 points out the design challenge and formally defines the problem and constraints. Section 4 details the proposed pin-count aware routing algorithm. Finally, sections 5 and 6 show our experimental results and conclusions.

2. PRELIMINARIES

This section first describes the related background of digital microfluidics and the EWOD chips. Then, the control mechanism of broadcast addressing is detailed.

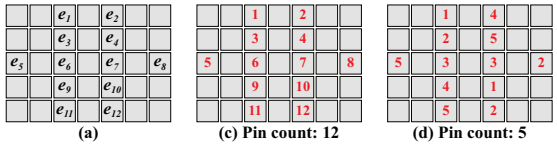
2.1 Digital Microfluidics and EWOD Chips

In recent microfluidic technology, liquids have been successfully discretized or *digitized* into independently controllable *droplets* in micro or nano scale. This miniaturization offers several advantages over the traditional continuous-flow or mist-based systems, such as higher sensitivity, lower reagent consumption, and more flexible controls. Moreover, the digitization allows complex microfluidic functions to be efficiently designed via hierarchical and cell-based design methods in modern VLSI automation.

In performing various fluidic-handling functions, a primary issue is the manipulation of droplets. Although droplets can be controlled on many driving platforms [13], the EWOD chips, also referred to as EWOD actuators, have received much more attention due to their high accuracy and efficiency, and simple fabrication [6]. The EWOD chip generates electric potential by actuating electrodes to change the wettability of droplets, such that droplets can be shaped and driven along the active electrodes [11, 12]. To induce enough change of wettability for droplet motion, the voltage value applied to electrodes must exceed a threshold. This phenomenon enables a binary value (i.e., 1/0) to represent a relatively logic-high/logic-low value of an actuation voltage, and thus the entire electrode controls can be modeled simply. Furthermore, by patterning electrodes to a general 2D array and adopting time-varying actuations, many droplet-based operations (e.g., mixing and cutting) can be well-performed on a 2D array in a *reconfigurable* manner [13].

2.2 Broadcast Addressing

To execute a specific bioassay, information for fluidic controls must be stored in the form of *electrode activation sequences*. Each bit in the sequence represents the activation status of the electrode in a specific time step, and can be represented as activated "1", deactivated "0", or don't care "X". The aforementioned, "1" ("0") represents a control signal with a relatively logic-high (logic-low) value of the actuation voltage. The symbol "X" indicates that the input signal can be either "1" or "0", which has no impact on scheduled fluidic controls [15]. Examples of an electrode set and the corresponding activation sequences are presented in Figures 4(a) and (b).



Electrode	e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9	e_{10}	e_{11}	e_{12}
Activation Sequence	1	1	0	0	0	X	X	0	X	X	X	X
	0	0	1	1	1	0	0	1	X	X	X	X
	0	0	0	0	0	1	1	0	0	0	X	X
	X	X	0	0	0	0	0	0	1	1	0	0
	X	X	X	X	1	0	0	1	X	X	1	1

(b)

Figure 4: (a) Electrodes that are used for handling fluidic functions. (b) Scheduled fluidic functions in the form of activation sequences. (c) Applies the direct-addressing scheme. (d) Applies the broadcast-addressing scheme.

To correctly drive these electrodes, control pins must be appropriately assigned to the electrodes for identifying input signals. This approach is also referred to as *electrode addressing*. Unlike direct addressing, where each electrode is assigned by an independent control pin, broadcast addressing focuses on electrode grouping and control signal merging through the compatibility of activation sequences. Specifically, each electrode activation sequence may contain several don't care terms. By carefully replacing these don't care terms with "1" or "0", multiple activation sequences can be merged to an identical outcome, which is also referred to as the *common compatible sequence* of these electrodes. Therefore, these electrodes can be assigned by the same control pin to receive the same control signal.

Take electrodes e_4 and e_5 in Figure 4(b) for example. By replacing "X" in the activation sequence of e_4 with "1", we can merge the activation sequences of e_4 and e_5 to "01001". Therefore, e_4 and e_5 can be addressed with the same control pin due to their mutually compatible activation sequences.

As the example in Figure 4, (c) and (d) respectively demonstrate the direct-addressing and broadcast-addressing outcomes. Compared with the direct-addressing result in (c), the broadcast-addressing result in (d) significantly reduces the required control pins from 12 to

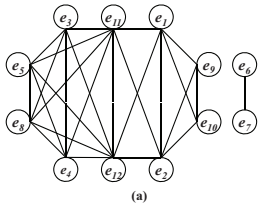
5. This reduction requires fewer electrical devices and connections to perform the same fluidic functions, thus improving chip reliability and reducing fabrication cost [15, 16]. Therefore, the derivation of a correct electrode-addressing result under the pin-constrained issue is of great importance, especially in the DMF marketplace.

3. PIN-CONSTRAINED CHIP DESIGN

This section first points out the difficulties and challenges for pin-constrained chip designs. Then, the practical constraints for broadcast addressing and routing are introduced. Finally, we formulate the design problem for EWOD chips.

3.1 Design Challenges

Typically, pin-constrained chip design consists of two major stages: (1) *broadcast-addressing stage* and (2) *routing stage*. In the broadcast-addressing stage, the major goal is to correctly address the electrodes with low pin-count demand. To this end, electrode grouping is introduced such that for all electrodes in any group, the corresponding activation sequences are mutually compatible. To specify this manner, a *compatibility graph* is constructed [15], where the vertex set represents the electrode set and an edge between two electrodes indicates their corresponding activation sequences are compatible. For example, Figure 5(a) demonstrates a compatibility graph G_c derived from Figure 4(b). Based on the compatibility graph, the electrode grouping can be mapped to the *clique partition problem*, which is a well-known example of an intractable problem in graph theory. Since each clique represents an electrode group with mutually compatible control signals, we can individually assign each clique with a dedicated control pin. Accordingly, by recognizing a minimum clique partition in the compatibility graph, the required number of control pins can be optimally minimized. However, the general minimum clique partition is known to be NP-hard [7] and thus is computationally expensive.



(a)

Two electrode grouping results		
Pin	Result 1	Result 2
1	e_1, e_{10}	e_1, e_2
2	e_3, e_8, e_{12}	e_3, e_4, e_8
3	e_6, e_7	e_6, e_7
4	e_2, e_9	e_9, e_{10}
5	e_4, e_5, e_{11}	e_5, e_{11}, e_{12}

(b)

Figure 5: (a) A compatibility graph G_c derived from Figure 4(b). (b) Two possible electrode grouping results.

After addressing, in the routing stage, wires must be appropriately routed to establish the correspondence between the control pins and the surrounding pads while minimizing the total wirelength. Hence, the routing problem for EWOD chips is similar to the typical escape routing, in which the objective is to individually route all terminal pins to the component (defined as 2D pin array) boundaries. However, in pin-constrained chip design, multiple electrodes may share the same control pin for pin-count reduction. In other words, a single signal source may contain multi-terminal pins. To realize the electrical connections, multi-terminal pins with the same control signal must first be wired together, and then escape to the component boundaries. This feature makes the typical two-pin-net based escape router unsuitable for the routing problem in EWOD chips. Therefore, a specialized escape routing algorithm must be developed to tackle this problem. Unfortunately, even simply routing for multi-terminal pins with minimum wirelength is also well-known to be NP-complete in most VLSI routing problems [4].

Although a number of heuristics and approximations can separately cope with the two design stages, the potential gap may result in an unsolvable routing problem. As discussed in Section 1, separate addressing and routing suffers from an infeasible routing solution, while the simultaneous method provides a higher-quality one (see Figure 2). The essence of this problem is that the clique partition is not unique and thus multiple electrode grouping results exist. To clarify these points, Figure 5(b) illustrates the corresponding electrode groups and addressing results of Figure 2 (result 1 for (a), and result 2 for (b)). Consequently, to achieve higher design performance, it is necessary to develop an integrated automation for pin-constrained designs. In this regard, the complexity resulting from the multi-objective minimization of pin count and wirelength has become the most difficult design challenge.

3.2 Broadcast Constraints

As discussed in Section 2.2: if a single control pin is assigned to an electrode set, all the corresponding activation sequences of these electrodes must be *mutually compatible*. Therefore, broadcast constraints (BC for short) can be formulated as the two following rules:

BC-Rule #1: Given an electrode set, if the corresponding activation sequences are mutually compatible, this electrode set can be addressed with the same control pin or not;

BC-Rule #2: Given an electrode set, if the corresponding activation sequences are not mutually compatible, this electrode set cannot be addressed with the same control pin.

3.3 Routing Constraints

Practically, the wiring connections and media substrate can be formed by using typical integrated circuit (IC) fabrication methods, or existing printed circuit board (PCB) manufacturing processes [3, 6]. In the IC industry, fabrication methods typically rely on thin film planar and photolithography, while the manufacturing processes of PCB are based on electroplating and multi-layer lamination [6]. Due to the distinct natures of these technologies, the different wiring criteria involve a variety of routing requirements and constraints. A primary difference is the wiring structures between the two technologies. In PCB-based manufacturing processes, wires can be routed in any angle or even in a rounded manner [1, 2], while the IC-based counterparts restrict most routing to be orthogonal. Thus, without loss of generality, we focus on orthogonal routing such that the horizontal and vertical properties can be realized in both IC-based and PCB-based technologies.

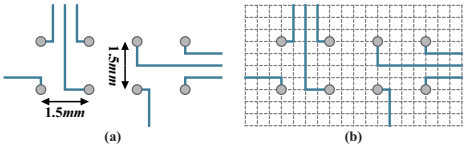


Figure 6: Number of wires between adjacent pins is 3. (a) Pin array. (b) Grid model.

Another significant consideration is the avoidance of electrical defects (e.g., shorts) caused by the shrinkage of wiring clearance. To prevent these faults, the spacing between wires must maintain a threshold; specifically, only a limited number of wires can pass through adjacent pins. Since the capacity between adjacent pins varies with the required electrode size for different bio-applications, it can thus be customized. In this paper, we use the real specification in [6] such that the maximum number of wires between adjacent pins is 3. As in most VLSI routing problems, we focus on uniform grid structure for flexibility and generality. Figure 6 exemplifies these concerns.

In addition, a multi-layer arrangement of electrical connections necessitates a mechanism for passing signals between layers (e.g., vias and contacts), raising a cost issue in both IC-based or PCB-based fabrication. For example, the cost of PCB prototype fabrication with one, two, four and six layers is respectively US$8.99, US$12.99, US$34.99 and US$59.99, resulting in expenses which increase exponentially with additional layers [1]. Since many biomedical applications prefer disposability, it is likely that using multi-layered chips is prohibitively expensive and thus undesirable. Therefore, in this paper, we focus on single-layer routing.

3.4 Problem Formulation

The pin-constrained design problem for an EWOD chip can be formulated as follows.

Input: *A set E_e of used electrodes for fluidic controls, control information of electrodes in the form of activation sequences, and chip specification.*

Constraint: *Both broadcast constraints and routing constraints should be satisfied.*

Objective: *Derive an electrode-addressing result and establish a routing solution, while minimizing the required control pins and wirelength.*

4. ALGORITHM

In this section, we present our pin-count aware routing algorithm. We first discuss the electrode grouping method used in our routing algorithm. Then, the pin-count aware global routing and progressive routing scheme are respectively detailed.

For the purpose of readability and clarity, we use a real-life chip application to exemplify each phase of the proposed algorithm. As illustrated in Figure 7(a), the chip for DMF based amino acid synthesis contains two types of droplets, functional droplets and wash droplets. The functional droplets (i.e., leucine, phenylalanine, and piperidine droplets) are used for amino acid synthesis, while the wash droplets are used for cleaning contaminations left behind on the surface, to avoid erroneous reaction outcomes. More details can be referred to [10].

4.1 Electrode Grouping Method

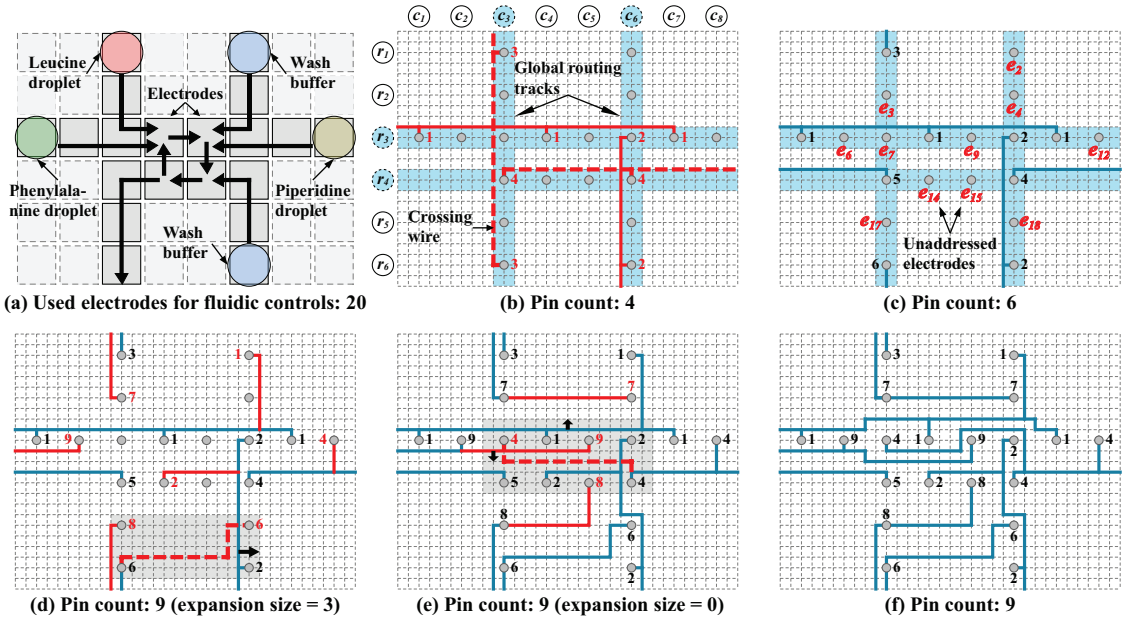


Figure 7: **This real-life chip describes each phase of the proposed pin-count aware routing algorithm. (a) DMF-based amino acid synthesis. (b) Constructs the global routing tracks by maximum-flow (MF) formulation to minimize the pin count. (c) Initial arrangement of control pins and wires after our pin-count aware global routing. (d)-(e) Progressive routing scheme with two subproblems. In each subproblem, the electrode addressing and routing are formulated to a minimum-cost maximum-flow (MCMF) network to minimize pin-count expansion. (f) Final arrangement of control pins and wires.**

In our pin-count aware routing algorithm, we focus on two kinds of electrode grouping methods in compatibility graph G_c, *maximum clique* and *maximum independent set*. By recognizing the maximum clique and maximum independent set in G_c, we can identify a maximum electrode group with mutually *compatible* and mutually *incompatible* control signals. Even though general recognitions of maximum clique and maximum independent set are known to be NP-hard, a number of high quality heuristics and approximation algorithms are available in the literature to solve them efficiently. In this paper, we use the heuristic in [8] as our electrode grouping method, which is based on the repeated addition of a candidate vertex with a defined indicator (i.e., vertex degree).

4.2 Pin-Count Aware Global Routing

The major goal of pin-count aware global routing is to schedule an initial arrangement for control pins and wires in a global view, while keeping the pin-count demand and wirelength minimized. To tackle the induced design complexity by simultaneous addressing and routing, we identify the factors that have impact on and attribute to pin-count demand and wirelength as follows.

1. As presented in Figure 8(a), if the control pins are not carefully assigned to electrodes, the induced routing complexity may trigger more deadlocks or detours between different control pins, implying the orientation of control pins and wires must be well-planned.
2. As presented in Figure 8(b), if the pins with the same control signal are oriented in a line, a straight wire can connect these pins together without any detour thereby reducing the wirelength.
3. As presented in Figure 8(c), once the orientation of a wire with a dedicated signal pin is determined, it is desirable to maximize the number of electrodes that can be wired together thereby reducing the pin count and wirelength.

To fully utilize the properties that are favorable for pin-count reduction and wirelength minimization, we construct the *global routing tracks* on rows and columns in the 2D pin array, such that all the electrodes can be covered. For each of these global routing tracks (i.e., a certain row or column), we identify a maximum electrode group without signal conflict and assign a dedicated control pin to this group. Then, on this track, conduction wires can be guided on a straight route to this control pin without any detour.

The proposed design technique provides two major advantages: (1) by performing electrode addressing and routing on these global routing tracks, design complexity can be considerably reduced from the whole 2D pin array to 1D orientation; (2) since control pins and wires are well-arranged on these specific tracks in a straight manner, the possibilities of routing detours and deadlocks can be minimized.

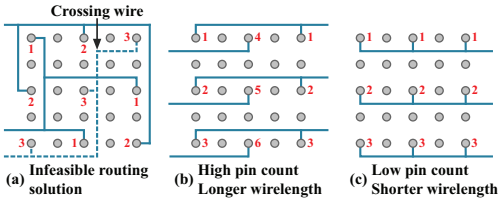


Figure 8: **Factors that impact the pin count and wirelength.**

4.2.1 Modeling the Global Routing Tracks Construction

Since each global routing track is assigned by a dedicated control pin, minimizing the pin-count demand requires minimizing the number of global routing tracks. Therefore, the problem for constructing global routing tracks can be formulated as follows.

Given: *A 2D pin array and an electrode set E_e.*

Objective: *Minimize the number of global routing tracks to cover E_e.*

As the example in Figure 9, the global routing tracks constructed in (a) require a total of 8 tracks (8 columns). Compared with (a), (b) leads to a better construction with a total of 5 tracks (1 row and 4 columns) to cover all electrodes.

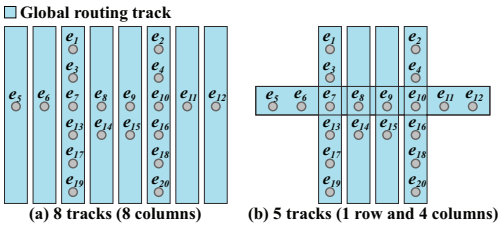


Figure 9: **Two feasible constructions for global routing tracks.**

4.2.2 Maximum-Flow Formulation

To solve the construction problem for global routing tracks, we construct a maximum-flow (MF) graph $G_{mf} = (V_{mf}, E_{mf})$ and propose two formulation rules. The first rule describes the formulation of V_{mf}, and the second rule describes the formulation of E_{mf}. The details of the two MF formulations rules are as follows.

MF-Rule #1: Formulation of V_{mf}

1. For each row i in the 2D pin array, create a node r_i.
2. For each column j in the 2D pin array, create a node c_j.
3. Create a source node s and a sink node t.

MF-Rule #2: Formulation of V_{mf}

1. For each node r_i, create a directed edge $s \rightarrow r_i$ with *one* unit capacity.
2. For each electrode $e_k \in E_e$ at row i and column j on the 2D pin array, create a directed edge $r_i \rightarrow c_j$ with *infinite* capacity.
3. For each node c_j, create a directed edge $c_j \rightarrow t$ with *one* unit capacity.

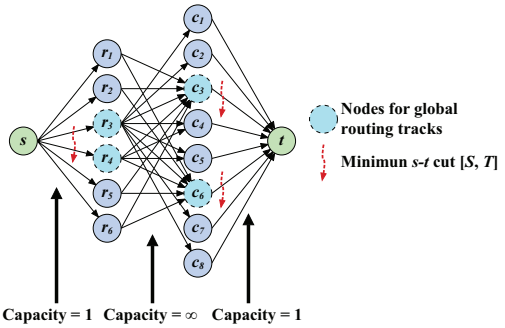


Figure 10: Example of the maximum-flow based global routing tracks construction for Figure 7(b).

As the example in Figure 7(b), there is a 2D pin array with 6 rows and 8 columns, and 20 electrodes used for fluidic controls. By implementing the two formulation rules, the entire flow network G_{mf} can be constructed as illustrated in Figure 10. Based on the two formulation rules, two theorems can be derived as follows.

THEOREM 1. *A minimum s-t cut in the flow graph G_{mf}, denoted as $[S, T]$, contains no edge $r_i \rightarrow c_j$.*

THEOREM 2. *The optimal number of global routing tracks is equal to the total of the capacities on the edge set $[S, T]$ in G_{mf}.*

In duality theorem, a maximum s-t flow value is equal to the minimum capacity of an s-t cut. Therefore, by deriving a maximum flow in G_{mf}, the minimum s-t cut $[S, T]$ can be obtained. Then, based on the two theorems, the global routing tracks can be optimally constructed by tracing the corresponding rows and columns of the node set $V_{[S,T]} - \{s, t\}$, where $V_{[S,T]}$ denotes the node set of $[S, T]$.

As shown in Figure 10, after deriving a maximum s-t flow, the red-dash arrows represent the edge set of a minimum s-t cut $[S, T]$, and the node set $V_{[S,T]} - \{s, t\}$ is $\{r_3, r_4, c_3, c_6\}$. By tracing the corresponding rows and columns in the 2D pin array, the global routing tracks can be constructed as illustrated in Figure 7(b).

4.2.3 Addressing and Routing

We use Figure 7(b)-(c) to exemplify our pin-count aware global routing. By deriving a maximum-flow (MF) formulation with the duality of min-cut property, the global routing tracks are constructed on row 3, row 4, column 3, and column 6, as presented in Figure 7(b). Based on the addressing and routing properties introduced in Figure 8, we iteratively select a global routing track with the largest non-conflicting electrode group on this track, and assign a dedicated control pin to this group, followed by guiding a horizontal/vertical wire to route these electrodes together, as shown in (b). In case of a crossing point, we identify the smallest electrode group and decompose it for readdressing and rerouting. For example, in (b), the routing for control pin 3 crosses the prerouted wire of control pin 1. Since our router tends to maximize the number of electrodes to share the same control pin, the smaller electrode group on column 3 (pin 3) is thus chosen to be decomposed for readdressing and rerouting. Finally, following pin-count aware global routing, an initial arrangement of control pins and wires can be obtained as illustrated in (c).

4.3 Progressive Routing Scheme

Although the pin-count aware global routing presented in the previous section can derive an electrode addressing and routing result, some electrodes may still not be addressed (see Figure 7(c)). Hence, in this routing stage, the major goal is to deal with these unaddressed electrodes left behind, while minimizing the increase of pin count and wirelength.

Motivated from [5], we present a progressive routing scheme based on *pin-count expansion* initiated from our global routing. The main idea is to divide the original problem into a set of manageable subproblems corresponding to each pin-count expansion. After every expansion, the entire electrode set is decomposed into two subsets, an unaddressed electrode set and an addressed electrode set. Our routing algorithm uses a network-flow based strategy to efficiently determine the minimum pin-count expansion for electrode addressing and routing between the two subsets. Then, the pin count is progressively and appropriately expanded until all electrodes are addressed and routed.

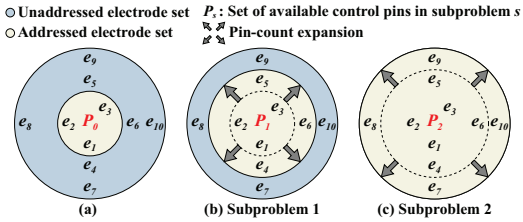


Figure 11: The basic concept of our progressive routing scheme.

The overall idea can be illustrated in Figure 11. (a) shows the set of available control pins initiated from our global routing, with an addressed electrode set and an unaddressed electrode set. For each subproblem, the pin count is minimally expanded for electrode addressing and routing as shown in (b). Finally, expansion ends when all electrodes are addressed (see (c)). Our progressive routing scheme offers three major advantages as follows.

1. Instead of directly solving the original problem, we focus on each manageably-sized subproblem thereby significantly reducing the entire design complexity.
2. By formulating the electrode addressing and routing into a flow network, the expansion of pin count can be minimally determined.
3. Our progressive routing also preserves the pre-scheduled addressing and routing result for successive expansions, without numerous modifications such as readdressing and rerouting.

4.3.1 Modeling the Pin-Count Expansion

The major challenge in our progressive routing scheme is to formulate the problem of pin-count expansion. The essence of pin-count expansion describes the concept of *extra* pin-count demand to realize the electrode addressing and routing for each subproblem s. However, to avoid pin-count overhead, the expansion size must be minimized. Hence, the means by which the set of available control pins in subproblem s, denoted as P_s, can be utilized is the major concern in modeling the pin-count expansion.

One of the difficulties in each subproblem s is to identify an unaddressed electrode set for addressing and routing. The difficulty is the potential interference between grouping unaddressed electrodes with addressed ones without violating broadcast constraints. For example, as depicted in Figure 12(a), if we directly solve all the addressing and routing problems between the addressed and unaddressed electrode sets, much of the compatibility needs to be examined for broadcast constraints and thus is computationally expensive. To tackle this problem, we reverse the regular electrode grouping method. Specifically, we identify a maximum unaddressed electrode group, denoted as E'_e, with mutually *incompatible*, rather than compatible, control signals. As demonstrated in Figure 12(b), this strategy achieves a significant reduction of complexity attributed to the omission of grouping considerations inside E'_e. In this manner, the addressing and routing problems can be regarded as a *one-to-one* matching determination between the two sets E'_e and P_s.

After an unaddressed electrode group E'_e is identified, the major goal is to appropriately schedule an electrode addressing and routing result. Since all electrodes $e_k \in E'_e$ must be independently addressed, unaddressed electrodes necessitate extra pin-count demand, implying a *pin-count expansion*. In order to avoid pin-count overhead, it is desirable to maximize the number of addressed electrodes by utilizing the existing control pins $p \in P_s$ such that the pin-count expansion can be minimized. Furthermore, the associated routing wirelength needs to be minimized. Consequently, for each subproblem s, the problem of pin-count expansion can be formulated as follows.

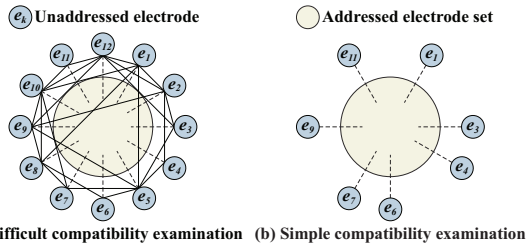


Figure 12: Compatibility between the unaddressed electrode set and the addressed electrode set. (a) Directly solves the addressing and routing with high design complexity. (b) Mutual incompatibility recognition ($E'_e = \{e_1, e_3, e_4, e_6, e_7, e_9, e_{11}\}$) with simple one-to-one matching.

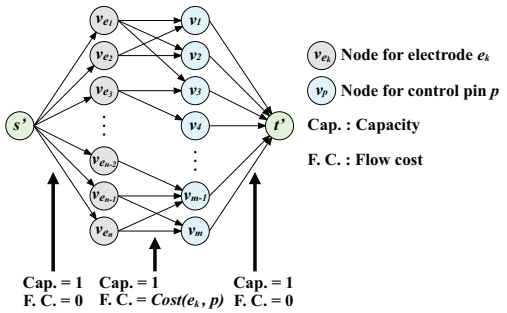


Figure 13: Formulates pin-count expansion to the minimum-cost maximum-flow network.

Given: *A 2D pin array, P_s, and E'_e.*

Constraint: *Broadcast constraints should be satisfied*

Objective: *Maximize the number of addressed electrodes by using P_s such that pin-count expansion is minimized, while also minimizing routing wirelength.*

4.3.2 Minimum-Cost Maximum-Flow Formulation

To minimize pin-count expansion, we construct a minimum-cost maximum-flow (MCMF) graph $G_{mcmf} = (V_{mcmf}, E_{mcmf})$ and propose two formulation rules. The first rule describes the formulation of V_{mcmf}, and the second rule describes the formulation of E_{mcmf}.

The key idea behind our MCMF formulation is to map the objective "*maximize the number of addressed electrodes by using P_s*" into "*maximum flow value*" in G_{mcmf}, with "*minimize the routing wirelength*" corresponding to "*minimum flow cost*". To avoid any violation of broadcast constraints in our MCMF formulation, we define the control pin set $P_s^k \in P_s$ for each electrode $e_k \in E'_e$ such that e_k can be addressed with the control pin $p \in P_s^k$. By identifying the compatibility between e_k and those addressed electrodes with control pins $p \in P_s$, the P_s^k can be obtained. Since the wirelength for routing an electrode e_k with the control pin $p \in P_s^k$ should be minimized, we define the routing cost as follows.

$$Cost(e_k, p) = \sum(\alpha \cdot g_c + \beta \cdot g_n), \forall e_k \in E'_e, p \in P_s^k \quad (1)$$

where $Cost(e_k, p)$ represents the pin-to-wire routing cost from electrode $e_k \in E'_e$ to the routed wire of control pin $p \in P_s^k$. Since our routing is based on uniform grid structure, if the routing for e_k crosses another wire in the grid point g_c, a high penalty α is assigned; otherwise a low cost β is assigned to the non-crossing grid point g_n. Then, we perform the A* maze searching method to find a minimum cost routing path. In this paper, we empirically set $\alpha = 10$ and $\beta = 0.1$.

The two MCMF formulations rules can be detailed as follows.

MCMF-Rule #1: Formulation of V_{mcmf}

1. For each electrode $e_k \in E'_e$, create a node v_{e_k}.
2. For each control pin $p \in P_s$, create a node v_p.
3. Create a source node s', and a sink node t'.

MCMF-Rule #2: Formulation of E_{mcmf}

1. For each node v_{e_k}, create a directed edge $s' \rightarrow v_{e_k}$ with *one* unit capacity and *zero* cost per unit flow.
2. For each node pair (v_{e_k}, v_p), where $e_k \in E'_e$ and $p \in P_s^k$, create a directed edge $v_{e_k} \rightarrow v_p$ with *one* unit capacity and $Cost(e_k, p)$ cost per unit flow.
3. For each node v_p, create a directed edge $v_p \rightarrow t'$ with *one* unit capacity and *zero* cost per unit flow.

Figure 13 shows a general diagram of the MCMF formulation. Based on the proposed MCMF formulation rules, we have the following two theorems

THEOREM 3. *A feasible $s' - t'$ flow represents a correct electrode addressing without any violation of broadcast constraints.*

THEOREM 4. *Based on the proposed MCMF network, we can adopt the MCMF algorithm to optimally maximize the number of addressed electrodes with minimum total routing costs.*

Based on the two theorems, we can maximize the number of addressed electrodes by deriving a maximum flow value in G_{mcmf} and have the following lemma.

LEMMA 1. *The extra pin-count demand for electrode addressing is equal to $|E'_e| - f_{mcmf}$, where f_{mcmf} denotes the maximum flow value in G_{mcmf}.*

4.3.3 Addressing and Routing

We use Figure 7(c)-(f) to clarify our progressive routing scheme. After pin-count aware global routing, an initial arrangement of control pins and wires can be shown in (c). The set of available control pins in (c), $P_1 = \{1, 2, 3, 4, 5, 6\}$, is the input pins of the first subproblem in the progressive routing scheme. Then we identify a maximum electrode group with mutually incompatible control signals, $E'_e = \{e_2, e_3, e_6, e_{12}, e_{14}, e_{17}, e_{18}\}$, from unaddressed electrode set. In the first subproblem, the goal is to utilize the set of available control pins, $P_1 = \{1, 2, 3, 4, 5, 6\}$, for addressing and routing the electrode group E'_e thereby minimizing the pin-count expansion. By formulating this issue into the MCMF network, a maximum addressing with minimum routing costs can be derived as shown in (d). In more detail, electrodes $\{e_2, e_{12}, e_{14}, e_{18}\}$ are respectively addressed using available control pins $\{1, 4, 2, 6\}$; while the electrodes $\{e_3, e_{17}, e_6\}$ are directly addressed with independent control pins $\{7, 8, 9\}$, implying a pin-count expansion with size 3. Since the routing cost in our MCMF network is estimated by minimum crossing points and wirelength, some wires may cross prerouted wires. For example, in (d), the red-dash wire for control pin 6 cannot be routed as it is blocked by the prerouted wire of control pin 2. For this crossing wire, we identify the encompassed bounding box enlarged by b unit as the rerouting region (see the shadow area in (d)). Empirically, b is initialized by 1 and will incrementally increase by one unit until it is routed successfully. Then, we iteratively choose a wire from the outer to the inner region, and route this wire along the outer region as much as possible to free more routing resources for inner wires. As the example in (d), the prerouted wire of control pin 2 will be rerouted along the outer region such that the crossing problem can be resolved.

After all electrodes $e_k \in E'_e$ are addressed and routed in the first subproblem, the pin count is progressively expanded by a minimal requirement (from 6 to 9). Then, our routing procedure seamlessly enters the subsequent subproblem initiated by the previous arrangement of control pins and wires. By adopting the same subroutine (see (e)), the entire solution of control pins and wires can eventually be obtained as shown in (f).

5. EXPERIMENTAL RESULTS

We implement the proposed algorithm in C++ language on a 2-GHz 64-bit Linux machine with 16GB memory. We evaluate our routing algorithm on a set of real-life chip applications [10, 13, 15] for amino-acid synthesis, protein synthesis, protein dilution, multiplexed assay, and multi-functional chip, as listed in Table I. To demonstrate our robustness, we simulate the fluidic-level synthesis in larger scale (e.g., at most 30 droplets and 150 electrodes) and randomly generate 7 hard test chips, as listed in Table I. For comparison purpose, we implement the direct addressing with maze routing, denoted as DA-maze, to independently route each electrode to component (2D pin array) boundary. To further show the performance of our integrated routing algorithm, we separately implement the broadcast addressing and routing, denoted as BA-maze. In BA-maze, we use the heuristic in [15] as the broadcast electrode-addressing manner. As discussed in Section 3.1, the routing problem for a broadcast-addressing result is an NP problem (multi-terminal pins routing). Therefore, we use a heuristic based on maze routing to sequentially and iteratively route a nearest electrode pair with the same control pin until all electrodes are routed.

Table I lists the overall comparison results. First, our algorithm shows better routability by completing 13 test cases out of 14 (92.9%), while the DA-maze and the BA-maze complete 7 (50.0%) and 8 (57.1%), respectively. In terms of the number of failed electrodes, our method outperforms the two methods by 4.5× and 13.3× better routability. This result demonstrates that our algorithm yields stronger routability on both real-life and hard test chips.

TABLE I: COMPARISON BETWEEN THE DA-MAZE, THE BA-MAZE, AND OUR ALGORITHM

Chip	Size	#E	Direct addressing				Broadcast addressing							
			DA-maze				BA-maze				Ours			
			#Pin	WL (#Grid)	#Fail	CPU time (sec.)	#Pin	WL (#Grid)	#Fail	CPU time (sec.)	#Pin	WL (#Grid)	#Fail	CPU time (sec.)
amino-acid-1	6 × 8	20	20	156	0	0.02	13	254	0	0.03	9	190	0	0.08
amino-acid-2	8 × 8	24	24	168	0	0.04	16	236	0	0.05	11	207	0	0.11
protein-1	13 × 13	34	-	-	1	-	19	814	0	0.43	24	462	0	0.26
protein-2	13 × 13	52	-	-	3	-	21	898	0	0.16	25	662	0	0.28
dilution	15 × 15	54	-	-	1	-	-	-	7	-	15	1178	0	0.17
multiplex	15 × 15	59	-	-	1	-	-	-	7	-	36	1444	0	0.36
multi-function	15 × 15	81	-	-	7	-	-	-	11	-	-	-	8	-
random-1	10 × 10	20	20	281	0	0.01	14	353	0	0.02	8	278	0	0.04
random-2	15 × 15	30	30	560	0	0.04	18	1053	0	0.05	11	614	0	0.10
random-3	20 × 20	60	-	-	1	-	23	4678	0	0.18	19	2720	0	0.31
random-4	30 × 30	90	90	8924	0	0.33	31	8558	0	0.37	26	5975	0	0.48
random-5	50 × 50	100	100	10945	0	1.19	-	-	23	-	37	7965	0	1.53
random-6	60 × 60	100	100	11344	0	1.48	-	-	27	-	41	8901	0	2.23
random-7	70 × 70	150	-	-	22	-	-	-	31	-	80	16612	0	6.65
Total					36				106				8	

#E: Number of used electrodes for fluidic controls. #Pin: Number of used control pins for electrode addressing.
#Fail: Number of failed electrodes (unable to find a valid addressing and routing manner).
WL: Total wirelength computed by the number of routing grids.

TABLE II: COMPARISON BETWEEN THE DA-MAZE AND OUR ALGORITHM

Chip	DA-maze			Ours		
	#Pin	WL (#Grid)	CPU time (sec.)	#Pin	WL (#Grid)	CPU time (sec.)
amino-acid-1	20	156	0.02	9	190	0.08
amino-acid-2	24	168	0.04	11	207	0.11
random-1	20	281	0.01	8	278	0.04
random-2	30	560	0.04	11	614	0.10
random-4	90	8924	0.33	26	5975	0.48
random-5	100	10945	1.19	37	7965	1.53
random-6	100	11344	1.48	41	8901	2.23
Total	384	32378	3.11	143	24130	4.57

TABLE III: COMPARISON BETWEEN THE BA-MAZE AND OUR ALGORITHM

Chip	BA-maze			Ours		
	#Pin	WL (#Grid)	CPU time (sec.)	#Pin	WL (#Grid)	CPU time (sec.)
amino-acid-1	13	254	0.03	9	190	0.08
amino-acid-2	16	236	0.05	11	207	0.11
protein-1	19	814	0.43	24	462	0.26
protein-2	21	898	0.16	25	662	0.28
random-1	14	353	0.02	8	278	0.04
random-2	18	1053	0.05	11	614	0.10
random-3	23	4678	0.18	19	2720	0.31
random-4	31	8558	0.37	26	5975	0.48
Total	155	16844	1.29	133	11108	1.66

Since the number of failed designs is different, it is hard to fairly perform a direct comparison between the two methods and ours in terms of pin count, wirelength, and runtime. Therefore, we focus on these chips which are completed by both our method and another approach as listed in Tables II and III. In the first comparison with DA-maze, Table II shows that our algorithm achieves 62.8% pin-count reduction and produce 25.5% shorter wirelength, with the reasonable CPU time. Compared with direct addressing, this result shows that the broadcast addressing requires only a small number of control pins to perform the same fluidic functions. Moreover, without complicated wiring connections, the system reliability and fabrication process can be significantly improved.

In the second comparison, we compare our integrated method with BA-maze which is based on separate broadcast addressing and routing, respectively in terms of pin count, wirelength, and runtime. As listed in Table III, we reduce the pin count by 14.2%, and shorten the wirelength by 34.1% with small increase of CPU time. By simultaneously considering the pin-count reduction and wirelength minimization, our method can effectively achieve greater design performance and higher-level integration.

6. CONCLUSION

In this paper, we have proposed the *first* pin-count aware routing algorithm to deal with the routing problem on broadcast electrode-addressing EWOD chips. Based on two kinds of flow formulations, *maximum-flow network* and *minimum-cost maximum-flow network*, the electrode addressing and routing problems can be correctly and effectively solved. By comprehensively integrating various pin-count saving issues into our routing, our router can lead to a superior addressing and routing solution with lower pin count, higher routability, and shorter wirelength to realize low-cost and reliable microfluidic actuators. Experimental results on real-life chip applications and hard test designs have demonstrated the robustness and scalability of our algorithm.

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